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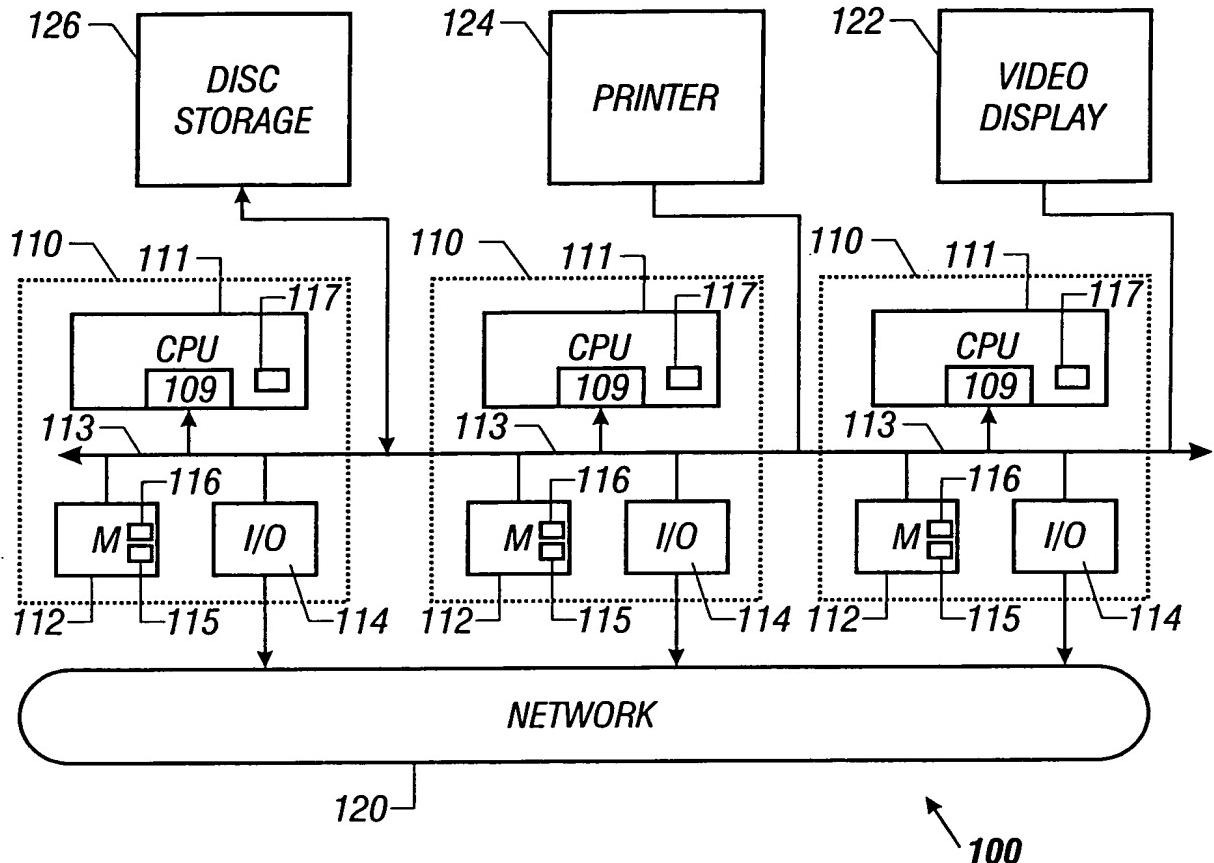


FIG. 1

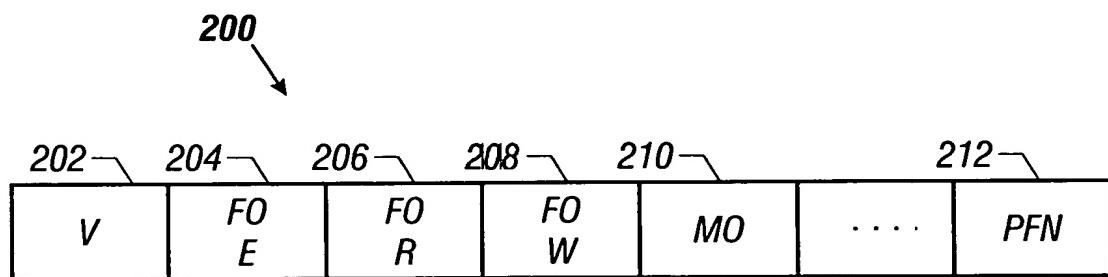


FIG. 2

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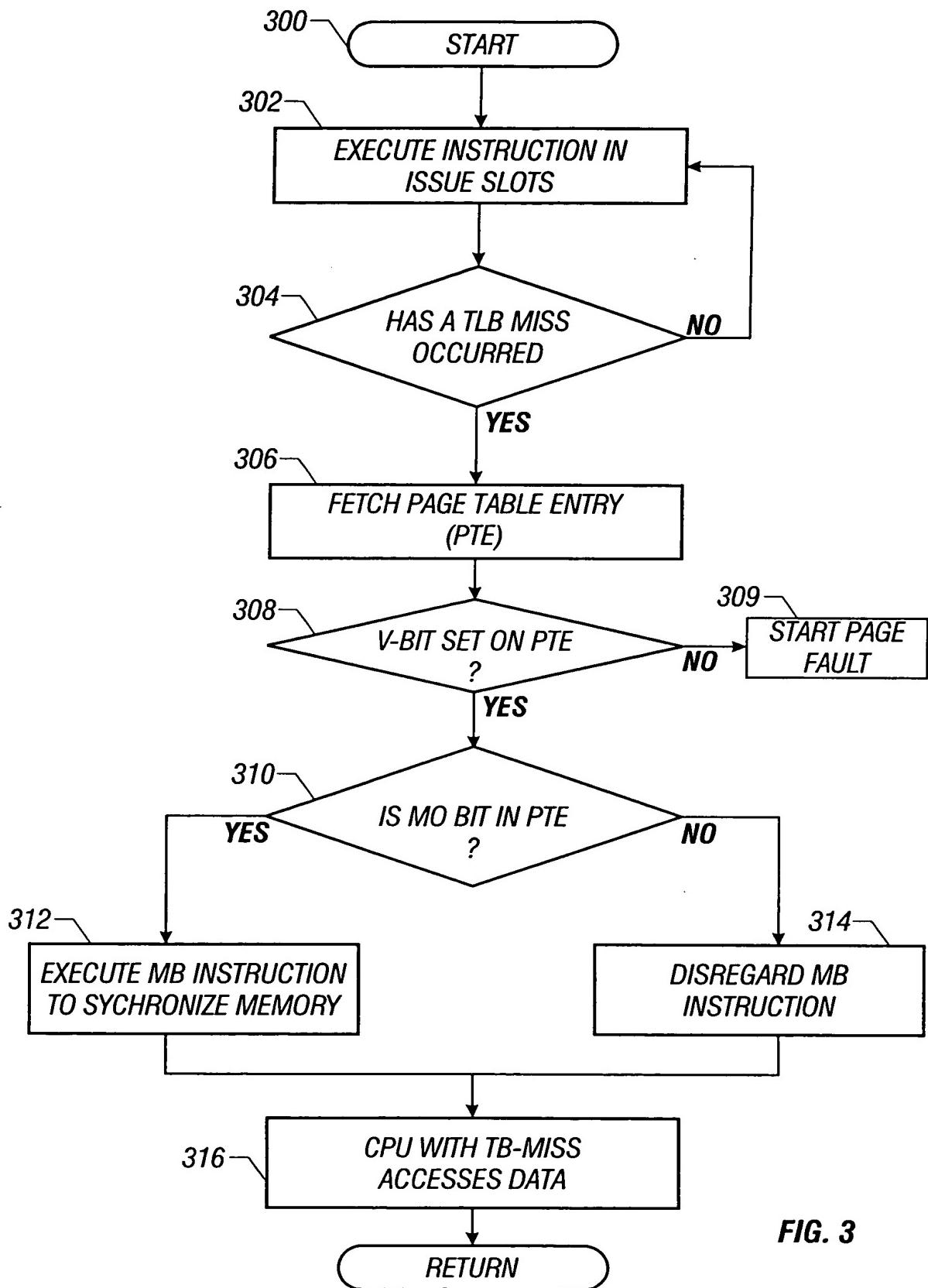


FIG. 3

The diagram illustrates a sequence of operations across four parallel timelines, one for each CPU (CPU1, CPU2, CPU3, CPU4). Each timeline is labeled '402' at its start. A bracket labeled '400' spans the fourth timeline. A dashed line labeled 'PTE' is positioned between the third and fourth timelines.

CPU1	CPU2	CPU3	CPU4
<i>INITIALIZE PAGE FRAME FOR ADDRESS VIRTUAL "FOO"</i>			<i>INITIALIZE PAGE FRAME FOR ADDRESS VIRTUAL "FOO"</i>
<i>MB</i>	<i>TBL MISS ON ADDRESS "FOO"</i>		<i>WRITE PTE FOR "FOO" WITH V-BIT SET AND MO BIT CLEAR</i>
<i>WRITE PTE FOR "FOO" WITH V-BIT SET AND MO BIT SET</i>	...		<i>TBL MISS ON ADDRESS "FOO"</i>
...	<i>FETCH PTE</i>		<i>FETCH PTE</i>
	<i>TEST MO AND ISSUE MB IF NEEDED</i>		<i>TEST MO AND BYPASS MB</i>
...

FIG. 4